Solutions - Homework 4

(Due date: April 2nd @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 pts)
- Design a counter using a Finite State Machine (FSM):
  - Counter features:
    - Count: 000, 001, 010, 011, 111, 110, 101, 100, 000, ...
    - resetn: Asynchronous active-low input signal. It initializes the count to “000”
    - input e: Synchronous input that increases the count when it is set to ‘1’.
    - output z: It becomes ‘1’ when the count is 111 or 100.

- Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (5 pts)

State Diagram and State Table:

State Assignment:
- S1: Q = 000
- S2: Q = 001
- S3: Q = 010
- S4: Q = 011
- S5: Q = 111
- S6: Q = 110
- S7: Q = 101
- S8: Q = 100

Excitation Table:

<table>
<thead>
<tr>
<th>E</th>
<th>Q2Q1Q0(t)</th>
<th>Q2Q1Q0(t+1)</th>
<th>z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 0</td>
<td>0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0 0 1</td>
<td>0 0 1</td>
<td>0</td>
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<tr>
<td>0</td>
<td>0 1 0</td>
<td>0 1 0</td>
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<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1 1 1</td>
<td>1 1 1</td>
<td>1</td>
</tr>
</tbody>
</table>

The output ‘z’ only depends on the present state ⇒ Moore FSM
- **Excitation equations and minimization**:

  \[ Q_2(t+1) = \bar{E}Q_2 + Q_1Q_2 + Q_0Q_2 + EQ_1\bar{Q}_0 \]

  \[ Q_1(t+1) = \bar{E}Q_1 + Q_1Q_0 + \bar{Q}_2Q_1 + EQ_2\bar{Q}_0 \]

  \[ Q_0(t+1) = \bar{E}Q_0 + E\bar{Q}_1\bar{Q}_0 + EQ_2(Q_1 + \bar{Q}_0) \]

  \[ z = \bar{Q}_1\bar{Q}_0Q_2 + Q_1Q_0Q_2 = Q_2(\bar{Q}_1\bar{Q}_0) \]

- **Circuit Implementation**:

![Circuit Diagram](image_url)
**PROBLEM 2 (15 PTS)**

- Sequence detector (with overlap):

  Draw the state diagram (both normal FSM representation and ASM chart) of a circuit (with an input $x$) that detects the following sequence: 00110101. The detector must assert an output $z$ when the sequence is detected.
PROBLEM 3 (30 PTS)

- Complete the timing diagram of the following FSM (represented as an ASM chart). (10 pts)
Complete the timing diagram of the following FSM. Is this a Mealy or a Moore machine? Why? (5 pts)

The output 'z' does not depend on the input 'x' \( \Rightarrow \) It is a Moore-type FSM.

Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (15 pts)

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity circ is
port ( clk, resetn: in std_logic;
       a, b: in std_logic;
       x,w,z: out std_logic);
end circ;

architecture behavioral of circ is

begin

Transitions: process (resetn, clk, a, b)
begin
if resetn = '0' then y <= S1;
elsif (clk'event and clk = '1') then
  case y is
  when S1 =>
    if a = '1' then
      if b = '1' then y <= S3; else y <= S1; end if;
    else
      y <= S2;
    end if;
  when S2 =>
    if a = '1' then y <= S3; else y <= S2; end if;
  when S3 =>
    if b = '1' then y <= S1; else y <= S3; end if;
  end case;
end if;
end process;

Outputs: process (y, a, b)
begin
  x <= '0'; w <= '0'; z <= '0';
  case y is
    when S1 => if a = '0' then z <= '1'; end if;
    when S2 => w <= '1';
    when S3 => if b = '1' then x <= '1'; end if;
  end case;
end process;
end behavioral;
```

**Problem 4 (20 pts)**
- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.

**Problem 5 (15 pts)**
- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project. You **must** use the provided template (Final Project - Report Template.docx).