VHDL Coding for FPGAs

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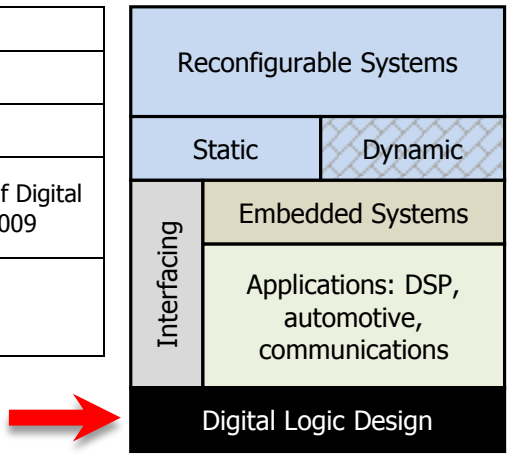
WEBPAGE	www.secs.oakland.edu/~llamocca/VHDLforFPGAs.html
REFERENCE	Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL Design", Third Edition, McGraw Hill, 2009
MATERIALS	Digilent Nexys-4 Artix-7 FPGA Development Board ISE Design Suite 14.7 - Webpack Edition



DESCRIPTION

- Digital Logic design with VHDL. VHDL description of logic gates, combinational circuits, synchronous sequential circuits, and finite state machines. VHDL testbench generation. Design Flow for CAD software. Introduction to Digital System Design with VHDL.

OUTLINE OF TOPICS

Introduction	▪ Design Flow: Design Entry, Functional Simulation, Mapping, Timing Simulation, Implementation ▪ Digital signal representation ▪ VHDL Description: Logic Gates ▪ VHDL Testbench Generation
Concurrent Description	▪ Concurrent statements: 'with-select', 'when-else' ▪ Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux.
Behavioral Description	▪ Asynchronous processes. ▪ Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux. ▪ Sequential statements: 'if-else', 'case', 'for-loop'
Structural Description	▪ Hierarchical design: port-map, for-generate, if-generate. ▪ Examples: Adder, multiplier, ALU, Look-up Table
Sequential Circuits	▪ Asynchronous processes: Latches ▪ Synchronous processes: flip-flops, counters, registers ▪ Testbench: generating clock stimulus
Finite State Machines	▪ VHDL Description of Finite State Machines ▪ Algorithmic State Machine (ASM) charts
Digital System Design	▪ Components of a digital system: datapath circuit, control circuits ▪ Examples: shift-and-add multiplier, bit-counting circuit, small processor, multiply and accumulate (MAC) circuit.
Parameterization	▪ Basic techniques ▪ Use of for-generate, if-generate, arrays in VHDL.
Fixed-point arithmetic	▪ Introduction to Fixed-point arithmetic ▪ Case example: Square root – Algorithmic description – Hardware implementation: iterative, pipelined