VHDL Coding for FPGAs

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MATERIALS    | Digilent Nexys-4/Nexys-4 DDR Artil-7 FPGA Development Board
             | ISE Design Suite 14.7 - Webpack Edition
             | Vivado HL 2016.2 Webpack Edition

DESCRIPTION
- Digital Logic design with VHDL. VHDL description of logic gates, combinational circuits, synchronous sequential circuits, and finite state machines. VHDL testbench generation. Design Flow for CAD software. Digital System Design with VHDL.

OUTLINE OF TOPICS

|                  | Digital signal representation
|                  | VHDL Description: Logic Gates
|                  | VHDL Testbench Generation
| Concurrent       | Concurrent statements: 'with-select', 'when-else' 
| Description      | Combinational circuits description: (priority) encoder, decoder, comparator, mux, de-mux.
| Behavioral       | Asynchronous processes.
| Description      | Behavioral description of Combinational circuits: (priority) encoder, decoder, comparator, mux.
| Structural       | Sequential statements: 'if-else', 'case', 'for-loop'
| Description      | Hierarchical design: port-map, for-generate, if-generate.
|                  | Examples: Adder, multiplier, ALU, Look-up Table
| Sequential       | Asynchronous processes: Latches
| Circuits         | Synchronous processes: flip-flops, counters, registers
|                  | Testbench: generating clock stimulus
| Finite State     | VHDL Description of Finite State Machines
| Machines         | Algorithmic State Machine (ASM) charts
| Digital System   | Components of a digital system: datapath circuit, control circuits
| Design           | Examples: shift-and-add multiplier, bit-counting circuit, small processor, multiply and accumulate (MAC) circuit.
|                  | Embedding counters and registers inside FSMs.
| Parameterization | Use of for-generate, if-generate.
|                  | Custom-defined data types, arrays in VHDL (e.g.: std_logic_2d), records.
|                  | Generic testbenches.
|                  | Packages in VHDL
| Miscellaneous    | I/O Text files:
| Topics           |  ▫ Synthesis: Reading input text files.
|                  |  ▫ Simulation: Reading input text files and writing output text files.
|                  |  ▫ Using Xilinx® primitives: BRAMs, XADCs, FIFOs, MMCMS, DSPs, etc.