

# Introduction to Vivado™

## OBJECTIVES

- ✓ Review VHDL Coding for FPGA and VHDL tesbenches.
- ✓ Learn the Xilinx FPGA Design Flow with the Vivado Webpack software: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream on the ZYBO Board.

## VHDL CODING

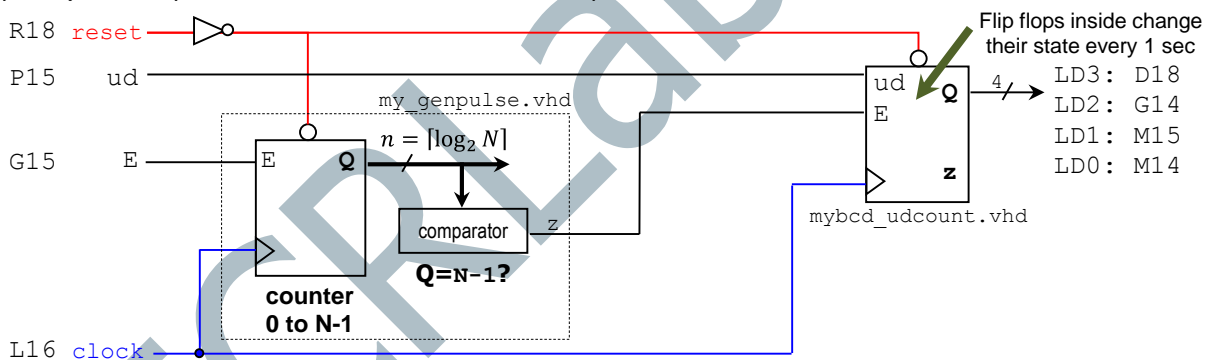
- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a tutorial and a comprehensive list of examples.

## ZYBO BOARD SETUP

- The ZYBO Board can receive power from the shared UART/JTAG USB port (J11). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- ZYBO documentation: Available in [class website](#).
- XDC file: The ZYBO Board manufacturers provide a template for all I/O ports in the Zynq SOC that are connected to peripherals in the ZYBO Board: `ZYBO_Master.xdc`.

## TEST PROJECT

- 4-bit up/down BCD counter.  $ud=1 \rightarrow 0, 1, 2, \dots, 9$ ,  $ud=0 \rightarrow 9, 8, 7, \dots, 0$ . The count changes every 1 second.
- **Inputs:** enable, reset, clock. **Outputs:** 4-bit count (connected to LEDs).
- **Hardware Design:** Even though the ZYNQ SoC contains a PS (Processing System) and a PL (Programmable Logic), this project is purely hardware:
  - ✓ Top file: `mybcd_udcount_top.vhd`. Top file.
  - ✓ Counter: `mybcd_udcount.vhd`. Up/down counter with enable.
  - ✓ Pulse generator: `my_genpulse.vhd`. This circuit generates a pulse (we can customize the interval of time between pulses). The output of this circuit is fed to the enable input of the counter.



- **ZYBO Board:** The frequency of the PL input clock is 125 MHz. The parameter  $N$  of the pulse generator is set so that it generates a pulse (of duration  $1/125$  us) every 1 s:

$$\frac{1}{125 \times 10^6} \times N = 1s \rightarrow N = 125 \times 10^6$$

## XILINX ZYNQ SOC (SYSTEM-ON-CHIP) DESIGN FLOW

- Create a new Vivado Project. Select the **ZYNQ XC7Z010-1CLG400C** device.
- Copy the hardware design files into the project folder and add them to the project. Synthesize your circuit (Run Synthesis).
- Add the top VHDL testbench to the project: `tb_mybcd_udcount_top.vhd`. Since  $N$  is a large number, only for simulation purposes, use  $N=10$ . You will need to re-execute all the steps here (except simulation) when you use the correct  $N$  value.
- Perform **Functional Simulation** (Run Simulation → Run Behavioral Simulation).
  - ✓ Tip: The tesbench file `tb_mybcd_udcount.vhd` is associated with `mybcd_udcount.vhd`. If you only want to simulate this file, first make sure to add and set this testbench as the top Simulation Source (Right-click on file → Set as Top)
- I/O Assignment: Get the `ZYBO_Master.xdc` file and uncomment the lines that contain the desired I/O assignments (the figure above indicates the SoC pin assignments). Replace the port signal names as required.
- Implement your design (Run Implementation).
- Perform **Timing Simulation** (Run Simulation → Post-Implementation Timing Simulation).
- Generate the bitstream file (Generate Bitstream).
- Download the bitstream on the ZYNQ SoC (Open Hardware Manager → Program Device) and test.