Embedded System Design for Zynq™ SoC

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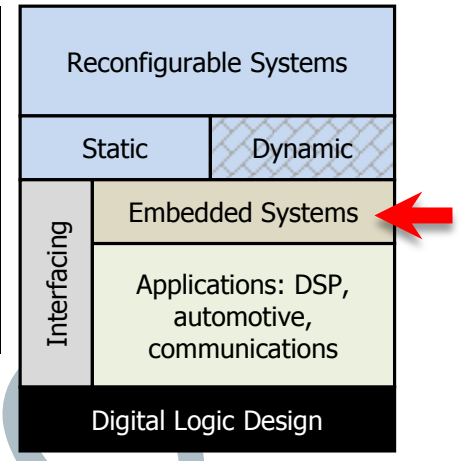
REFERENCES	▪ Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, "*The Zynq Book Tutorials*", v.1.2, Sep. 2014. ✓ Free download: http://www.zynqbook.com/
MATERIALS	ZYBO Zynq™-7000 Development Board Vivado™ Design Suite 2016.2 – Webpack Edition Xilinx Software Development Kit 2016.2



DESCRIPTION

- Embedded System Design with Vivado™ Design Suite software for Zynq™ System-on Chip. Software implementation with the Software Development Kit (SDK). Hardware/software co-design: creation of custom-defined VHDL IP cores, interfacing with the AXI bus, and creating software applications to control the VHDL IP cores.

OUTLINE OF TOPICS

Introduction to Vivado	▪ Hardware Design Flow: Design Entry, Functional Simulation, Mapping, Timing Simulation, Implementation ▪ Case example: Counter with enable controlled by a pulse generator ✓ I/O assignment: XDC file ✓ VHDL Testbench Generation and Testing
Introduction to Hardware/Software Design	▪ Using both the PL (Programmable Logic) and PS (Processing System). ▪ Vivado: Create a block-based project. Use of AXI GPIO peripheral to control LEDs ▪ SDK: Create a software application.
AXI4-Lite: Custom Peripheral	▪ Case example: Pixel Processor ▪ Vivado: Create block-based project. Create IP. Simple AXI interface ▪ SDK: Load custom drivers. Create software application and test with UART.
	▪ Case example: Pipelined Divider ▪ Vivado: Create block-based project. Create IP. Complex AXI interface ▪ SDK: Load custom drivers. Create software application and test with UART.
AXI4-Full: Custom Peripheral	▪ Case example: Pixel Processor ▪ Vivado: Create block-based project. Create IP. AXI4-Full Interface. ▪ Case examples: AXI DCT 2-D, cordic, sqrt
	▪ Case example: DCT or Matrix multiplier (with a constant matrix) ▪ Vivado: Create block-based project. Create IP. Complex AXI interface ▪ SDK: Load custom drivers. Create software application and test with UART.
Using the SD Card (in PS)	▪ Software drivers ▪ Reading/writing binary and text files.
Dynamic Partial Reconfiguration (PL)	▪ Vivado Design Flow using TCL scripts. ▪ Case example: LED Pattern controller ▪ Testing with JTAG interface.
Dynamic Partial Reconfiguration (PL+PS)	▪ Vivado Design Flow using TCL script for PS+PL ▪ Case example: Pixel Processor ▪ Case example: DCT 2D ▪ SDK: Write partial bitstreams using the PCAP port.
AXI4-Stream: Custom Peripheral	▪
Using DMA	▪
Applications	▪ HDMI, Audio