Solutions - Final Exam

(December 8th @ 7:00 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 pts)
- Given the following circuit, complete the timing diagram.
  The LUT 6-to-6 implements the following function: OLUT = ceil(sqrt(ILUT)), where ILUT is a 6-bit unsigned number.
  For example ILUT = 35 (100011₂) → OLUT = ceil(sqrt(35)) = 6 (000110₂)

PROBLEM 2 (12 pts)
- Complete the timing diagram of the following circuit. G = G₃G₂G₁G₀ = 1001, Q = Q₃Q₂Q₁Q₀
**Problem 3 (22 pts)**

- Sequence detector: The machine has to generate \( z = 1 \) when it detects the sequence 1011. Once the sequence is detected, the circuit looks for a new sequence.
- The signal \( E \) is an input enable: It validates the input \( x \), i.e., if \( E = 1 \), \( x \) is valid, otherwise \( x \) is not valid.

**State Diagram, State Table, and Excitation Table:**

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>( z )</th>
</tr>
</thead>
<tbody>
<tr>
<td>00,01,10/0</td>
<td>00,01,11/0</td>
<td>00,01,11/0</td>
</tr>
<tr>
<td>00,01,10/0</td>
<td>00,01,10/0</td>
<td>00,01,10/0</td>
</tr>
</tbody>
</table>

**Ex/z**

- **resetn** = 0
- **S1**: \( Q = 00 \)
- **S2**: \( Q = 01 \)
- **S3**: \( Q = 10 \)
- **S4**: \( Q = 11 \)

**State Assignment:**

- \( S1: Q = 00 \)
- \( S2: Q = 01 \)
- \( S3: Q = 10 \)
- \( S4: Q = 11 \)

This is a Mealy Machine. The output \( z \) depends on the input as well as on the present state.

**Excitation equations, minimization, and circuit implementation:**

- \( Q_1(t+1) = EQ_1 + EQ_0 + xQ_1Q_0 \)
- \( Q_0(t+1) = EQ_0 + EQ_0 + xQ_1Q_0 \)
- \( z = EQ_1Q_0 \)

**State Diagram**: (any representation), State Table, and the Excitation Table of this circuit with inputs \( E \) and \( x \) and output \( z \). Is this a Mealy or a Moore machine? Why? (15 pts)

**Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (4 pts)**

**Sketch the circuit. (3 pts)**
PROBLEM 4 (20 PTS)

- Complete the timing diagram of the circuit shown below: (8 pts)

- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (12 pts)

\[ Q_1(t+1) = (Q_1 + Q_0) \oplus w \]
\[ Q_0(t+1) = Q_1Q_0w \]
\[ z = wQ_1Q_0 \]

State Assignment:
S1: Q=00  S2: Q=01  
S3: Q=10  S4: Q=11

<table>
<thead>
<tr>
<th>PRESENT STATE</th>
<th>NEXTSTATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( w )  ( Q_1Q_0(t) )</td>
<td>( Q_1Q_0(t+1) )  ( z )</td>
</tr>
<tr>
<td>0  0  0</td>
<td>1  0  0</td>
</tr>
<tr>
<td>0  0  1</td>
<td>0  0  0</td>
</tr>
<tr>
<td>0  1  0</td>
<td>0  0  0</td>
</tr>
<tr>
<td>0  1  1</td>
<td>0  0  0</td>
</tr>
<tr>
<td>1  0  0</td>
<td>0  1  0</td>
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<td>1  0  1</td>
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<tr>
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<td>1  1  1</td>
</tr>
<tr>
<td>1  1  1</td>
<td>1  0  0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PRESENT STATE</th>
<th>NEXT STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( w )</td>
<td>( Q_0 )</td>
</tr>
<tr>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>0</td>
<td>S2</td>
</tr>
<tr>
<td>0</td>
<td>S3</td>
</tr>
<tr>
<td>0</td>
<td>S4</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>S2</td>
</tr>
<tr>
<td>1</td>
<td>S3</td>
</tr>
<tr>
<td>1</td>
<td>S4</td>
</tr>
</tbody>
</table>

\[ \text{resetn} = 0 \]
PROBLEM 5 (16 PTS)
- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( clk, resetn: in std_logic;
         r, p, q: in std_logic;
         x, w, z: out std_logic);
end circ;

architecture behavioral of circ is
  type state is (S1, S2, S3);
  signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
    if resetn = '0' then
      y <= S1;
    elsif (clk'event and clk = '1') then
      case y is
        when S1 =>
          if r = '1' then
            y <= S2;
          else
            if p = '1' then
              y <= S3;
            else
              y <= S1;
            end if;
          end if;
        when S2 =>
          if p = '1' then
            y <= S1;
          else
            y <= S3;
          end if;
        when S3 =>
          if q = '1' then
            y <= S3;
          else
            y <= S2;
          end if;
      end case;
      end if;
  end process;
  Outputs: process (y, r, p, q)
  begin
    x <= '0'; w <= '0'; z <= '0';
    case y is
      when S1 =>
        if r = '0' then
          if p = '0' then
            w <= '1'; x <= '1';
          end if;
        end if;
      when S2 =>
        if q = '0' then
          x <= '1';
        if p = '0' then
          z <= '1';
        end if;
      when S3 =>
        if q = '0' then
          x <= '1';
        end case;
    end process;
  end behavioral;

This is a Mealy Machine. The outputs \(x, w, z\) depend on the input as well as on the present state.

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**Problem 6 (18 pts)**

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.

![Timing Diagram](image-url)