PROBLEM 1 (30 PTS)
- Draw the state diagram (in ASM form) of the FSM whose VHDL description is listed below:

```vhdl
classic ieee;
use ieee.std_logic_1164.all;
entity circ is
  port (clk, rstn: in std_logic;
    a, b: in std_logic;
    x, w, z: out std_logic);
end circ;
architecture behavioral of circ is
  type state is (S1, S2, S3);
signal y: state;
begin
  Transitions: process (rstn, clk, a, b)
  begin
    if rstn = '0' then
      y <= S1;
    elsif (clk'event and clk = '1') then
      case y is
        when S1 =>
          if a = '1' then y <= S2;
          else if b = '1' then y <= S3; else y <= S1; end if;
        end if;
        when S2 =>
          if a = '1' then y <= S2; else y <= S1; end if;
        when S3 =>
          if b = '1' then y <= S3; else y <= S1; end if;
      end case;
    end if;
  end process;
  Outputs: process (y, a, b)
  begin
    x <= '0'; w <= '0'; z <= '0';
    case y is
      when S1 => if a = '1' then z <= '1'; end if;
      when S2 => s <= '1';
      when S3 => w <= '1';
    end case;
  end process;
end behavioral;
```

PROBLEM 2 (40 PTS)
- Complete the timing diagram of the following FSM (represented in ASM form):

![Timing Diagram]

PROBLEM 3 (30 PTS)
- Sequence detector (with overlap): Draw the state diagram (in ASM mode) of a circuit that detects the following sequence: 0110. The detector must assert an output $z = 1$ when the sequence is detected.