Homework 4
(Due date: November 17th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (15 pts)
- Complete the timing diagram of the following circuit. \( G = G_3G_2G_1G_0 = 1101 \), \( Q = Q_3Q_2Q_1Q_0 \)

PROBLEM 2 (20 pts)
- Design a counter using a Finite State Machine (FSM):
  - Counter features:
    - Count: 000, 010, 100, 001, 011, 101, 111, 000, 010, 100, ...
    - \( \text{resetn} \): Asynchronous active-low input signal. It initializes the count to '000'.
    - \( \text{E} \): Synchronous input that increases the count when it is set to '1'.
    - output \( z \): It becomes '1' when the count is 111.
  - Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
  - Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
  - Sketch the circuit. (5 pts)

PROBLEM 3 (30 pts)
- Sequence detector: Provide the State Diagram (any representation) and the Excitation Table of a circuit with an input \( x \) and output \( z \). The machine has to generate \( z = 1 \) when it detects the sequence 0110101. Right after the sequence is detected, the circuit looks for a new sequence. (10 pts).
  - The signal \( E \) is an input enable: It validates the input \( x \), i.e., if \( E = 1 \), \( x \) is valid, otherwise \( x \) is not valid. The figure below illustrates the behavior for a certain input stream.
Complete the timing diagram of the following FSM. Is this a Mealy or a Moore machine? Why? (5 pts)

Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (15 pts)

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity circ is
    port ( clk, resetn, a, b: in std_logic;
           x, w, z: out std_logic);
end circ;

architecture behavioral of circ is
    type state is (S1, S2, S3);
signal y: state;

begin
    Transitions: process (resetn, clk, a, b)
    begin
        if resetn = '0' then
            y <= S1;
        elsif (clk'event and clk = '1') then
            case y is
                when S1 =>
                    if a = '1' then
                        if b = '1' then y <= S3; else y <= S1; end if;
                    else
                        y <= S2;
                    end if;
                when S2 =>
                    if b = '1' then y <= S3; else y <= S2; end if;
                when S3 =>
                    if a = b then z <= '1'; else y <= S1; end if;
            end case;
        end if;
    end process;

    Outputs: process (y, a, b)
    begin
        x <= '0'; w <= '0'; z <= '0';
        case y is
            when S1 => if a = '1' then x <= '1'; end if;
            when S2 => w <= '1';
            when S3 => if a = b then z <= '1'; end if;
        end case;
    end process;
end behavioral;
```
PROBLEM 4 (20 PTS)

- Complete the following timing diagram (A and P are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.

Register (for \( \overline{E} \)): \( \overline{sclr} \) synchronous clear. Here, if \( \overline{sclr} = E = 1 \), the register contents are initialized to 0.

Parallel access shift registers (for \( A \) and \( B \)): If \( E = 1 \): \( s,l = 1 \rightarrow \text{Load} \), \( s,l = 0 \rightarrow \text{Shift} \)

PROBLEM 5 (15 PTS)

- Attach a printout of your Project Status Report (no more than two pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (Final Project – Report Template.docx).