System Considerations

- Interfacing
- Performance
- Power
- Size
- Ease-of Use
  - Programming
  - Interfacing
  - Debugging
- Cost
  - Device cost
  - System cost
  - Development cost
  - Time to market
- Integration
  - Memory
  - Peripherals
Different Needs? Multiple Families!

Lowest Cost
Control Systems
- Motor Control
- Storage
- Digital Ctrl Systems

C2000
(C20x/24x/28x)
- 'C1x 'C2x

C5000
(C54x/55x)
- 'C5x

Efficiency
Best MIPS per Watt / Dollar / Size
- Wireless phones
- Internet audio players
- Digital still cameras
- Modems
- Telephony
- VoIP

Max Performance with Best Ease-of-Use
- Multi Channel and Multi Function App's
- Comm Infrastructure
- Wireless Base-stations
- DSL
- Imaging
- Multi-media Servers
- Video
What Problem Are We Trying To Solve?

Digital sampling of an analog signal:

Most DSP algorithms can be expressed with MAC:

\[ Y = \sum_{i=1}^{\text{count}} a_i * x_i \]

for (i = 1; i < count; i++){
    sum += m[i] * n[i];
}
Fast MAC using only C

Multiply-Accumulate (MAC) in Natural C Code

```c
for (i = 0; i < count; i++){
    sum += m[i] * n[i];
}
```

- Fastest Execution of MACs
  - The ‘C6x roadmap ... from 200 to 2400 MMACs

- Ease of C Programming
  - Even using natural C, the ‘C6000 Architecture can perform 2 to 4 MACs per cycle
  - Compiler generates 80-100% efficient code

How does the ‘C6000 achieve such performance from C?
Fastest MAC using Natural C

float mac(float *m, float *n, int count)
{
    int i, float sum = 0;
    for (i = 0; i < count; i++) {
        sum += m[i] * n[i];
    }
    ...
}

LOOP: ; PIPED LOOP KERNEL
LDDW .D1 A4++,A7:A6
LDDW .D2 B4++,B7:B6
MPYSP .M1X A6,B6,A5
MPYSP .M2X A7,B7,B5
ADDSP .L1 A5,A8,A8
ADDSP .L2 B5,B8,B8
[A1] B .S2 LOOP
[A1] SUB .S1 A1,1,A1
'C6000 System Block Diagram

Looking at the internal buses ...
‘C6000 Internal Buses

- **Internal Memory**
  - Program Addr x32
  - Program Data x256
  - Data Addr - T1 x32
  - Data Data - T1 x32/64
  - Data Addr - T2 x32
  - Data Data - T2 x32/64

- **External Memory**
  - DMA Addr - Read
  - DMA Data - Read
  - DMA Addr - Write
  - DMA Data - Write

- **A regs**
- **B regs**
- **PC**
- **DMA**
Next, the internal memory ...
‘C6711 Memory

- 4K Program Cache
- 4K Data Cache
- 64K Prog / Data (Level 2)
- CPU

64KB Internal

0000_0000

On-chip Peripherals

0180_0000

128MB External

2

8000_0000

128MB External

1

9000_0000

128MB External

0

A000_0000

128MB External

2

B000_0000

128MB External

3

FFFF_FFFF

128MB External

3
Looking at each peripheral ...
**External Memory Interface (EMIF)**

- Glueless access to async/sync memory
- Works with PC100 SDRAM (cheap, fast, and easy!)
- Byte-wide data access
- 16, 32, or 64-bit bus widths

**Register Set A**

**Register Set B**

**Internal Buses**

**Async**

**SDRAM**

**SBSRAM**

**Internal Memory**

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Parallel Peripheral Interface

**HPI:** Dedicated, slave-only, async 16/32-bit bus allows host-μP access to C6000 memory

**XBUS:** Similar to HPI but provides …
- Master/slave and sync modes
- Glueless i/f to FIFOs (up to single-cycle xfer rate)

**PCI:** Standard 32-bit, 33MHz PCI interface

These interfaces provide means to bootstrap the C6000
General Purpose Input/Output (GPIO)

- 'C64x provides 8 or 16 bits of general purpose bitwise I/O
- Use to observe or control the signal of a single-pin
McBSP and Utopia

Multi-Channel Buffered Serial Port (McBSP)
- 2 (or 3) full-duplex, synchronous serial-ports
- Up to 100 Mb/sec performance
- Supports multi-channel operation (T1, E1, MVIP, …)

Utopia (C64x)
- ATM connection
- 50 MHz wide area network connectivity
Direct Memory Access (DMA / EDMA)

- Transfers any set of memory locations to another
- 4 / 16 / 64 channels (transfer parameter sets)
- Transfers can be triggered by any interrupt (sync)
- Operates independent of CPU
- On reset, provides bootstrap from memory
Timer / Counter

- Two (or three) 32-bit timer/counters
- Can generate interrupts
- Both input and output pins
Turbo Coprocessor (TCP)
- Supports 35 data channels at 384 kbps
- 3GPP / IS2000 Turbo coder
- Programmable parameters include mode, rate and frame length

Viterbi Coprocessor (VCP)
- Supports >500 voice channels at 8 kbps
- Programmable decoder parameters include constraint length, code rate, and frame length
PLL

- External clock multiplier
- Reduces EMI and cost
- Pin selectable

Input
- CLkin

Output
- CLKOUT1
  - Output rate of PLL
  - Instruction (MIP) rate
- CLKOUT2
  - 1/2 rate of CLKOUT1
C6000 Roadmap

Software Compatible

Floating Point

Multi-core

C64x™ DSP
1.1 GHz

C6414
C6415
C6416

2nd Generation

General Purpose

C64x™ DSP

C6414
C6415
C6416

1st Generation

Highest Performance

C64x™ DSP

C6201
C6202
C6203
C6204
C6205
C6211

C6701
C6711
C6712
C6713

3G Wireless Infrastructure

Media Gateway

1st Generation

Highest Performance

C62x™

C67x™

Time