Introduction to FPGA

SUBRA GANESAN
Embedded system Characteristics

- Need increase in performance and more functions often.
- Need Integration of more devices and chips
- Decrease in Power consumption
- Decrease in cost
- Decrease in size
- Decreased time to market
Implement using?

Microprocessor/ Microcontroller -- more commonly used.

ASIC -- for large volume products

FPGA -- How easy or How fast?
Advantages of Micros

• Flexible to program and change
• Available off the shelf as processor, board, or with interface chips
• You can choose from 100s of types of Micros to suit the application
• Easy to bring out a product in a short time
• Power consumption is medium
• Custom board can be designed after developing the product using generic boards.
Micros-- Disadvantages

- If you change the requirement or processor, a new board is needed.
- Micro may contain more features than needed or may not have needed features.
- Cost depends on the volume.
- To increase performance, you need to increase the memory or change the processor etc.
ASIC--- Advantage

- Lowest per unit cost for high volume
- Can optimize power consumption, speed, performance, size, etc
- Initial development cost prevents others entering this market.
ASIC– Disadvantage

- Initial Cost is high and increases every year
- High Labor cost to design, test, modify etc
- Development is challenging
- Complex
- Becomes obsolete soon since technology or requirement changes.
FPGA-- Advantages

- You can reconfigure the design
- True parallelism
- High speed
- Costs less than ASIC for medium volume
- Once this product works satisfactorily, you can make ASIC later.
- A number of FPGA devices available to suit the applications.
- Development tools cost is nominal.
FPGA disadvantage

- Internal Memory is limited
- Analog interface is challenging
- Power consumption is more
- Difficult to program compared to Micro
- Cost is more than micro cost
- Not Suitable for small volume product
- Learning to use or design Complex FPGA is more challenging
FPGA, Micro, ASIC cost

The graph illustrates the cost comparison between FPGA, Micro, and ASIC across different series and volumes. Each series (Series 1 to Series 4) shows a trend in cost increase with volume.
FPGA Vendors

- Actel
- Altera
- Atmel
- Lattice
- QuickLogic
- Xilinx
Future of FPGA in Embedded System

- Price of Complex FPGAs with 32-bit soft microprocessor core are now falling and will be close to microprocessor system price in 5 years.
- Altera, Xilinx have a number of devices for Embedded system market at different price ranges.
- FPGA represent the logical extension in the Hard to Soft migration of system functionality.
- Soft design methods, tools are growing.
- Processors, peripheral devices, logic, software can all be changed in FPGA system even after manufacture.
FPGA Design needs System Approach

- FPGA is a configurable platform.
- You can move some functions to hardware or to software easily in FPGA for optimal performance. Example: Add more features to the mobile phone FPGA core.
- Schematic based FPGA development. Example: Matlab, Labivew provide FPGA support
Glossary for FPGA devices

- FPGA --- Field Programmable Gate Array
- FPSC-- Field Programmable System Chip (Processor Core + FPGA)
- FPAA-- Field Programmable Analogue Array (Anadigm)
- PAC-- Programmable Analog IC (lattice semiconductor)
- PLD -- Programmable logic device
- CPLD-- Complex Programmable Logic Device
- SPLD -- Simple Programmable logic device
- EPLD -- Erasable programmable logic device
- PAL -- Programmable Array Logic
- PLA -- Programmable Logic Array
- PsoC- Programmable System on Chip
- LCA --- Logic Cell Array (Xilinx FPGA)
- GAL- Generic Array Cell (TM Lattice)
Reference: Brown and Vranesic Book on Digital design

Figure 3.24  Programmable logic device as a black box.
Figure 3.25. General structure of a PLA.
Figure 3.26. Gate-level diagram of a PLA.

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Figure 3.27. Customary schematic for the PLA in Figure 3.26.
Figure 3.28. An example of a PLA.
Figure 3.29. Extra circuitry added to OR-gate from Figure 3.28.
Figure 3.30. A PLD programming unit (courtesy of Data IO Corp).
Figure 3.31. A PLCC package with socket.
Figure 3.32. Structure of a complex programmable logic device (CPLD).
Figure 3.33. A section of the CPLD in Figure 3.32.
Figure 3.34. CPLD packaging and programming.
Figure 3.36. A two-input lookup table (LUT).

(a) Circuit for a two-input LUT

(b) \( f_1 = \overline{x}_1 \overline{x}_2 + x_1 x_2 \)

(c) Storage cell contents in the LUT
Figure 3.37. A three-input LUT.
Figure 3.40. A section of two rows in a standard-cell chip.
Figure 3.41. A sea-of-gates gate array.
Figure 3.65. Programmable version of a NOR-NOR PLA.

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Figure 3.66. A NOR-NOR PLA used for sum-of-products.
Figure 3.67. PAL programmed to implement two functions in Figure 3.66.
Figure 3.68. Pass-transistor switches in FPGAs.
Figure 4.18. Implementation in a CPLD.
Figure 4.19. Implementation in an FPGA.